IN THE CLAIMS

Please amend the claims as follows:

1. A circuit for calculating a discriminating function with successive iterations and with a work register on data divided into blocks, comprising:

a single operator ~~(2)~~ in wired logic for executing the function;

a plurality of work registers ~~(3)~~ sharing said operator, each register sotring a current state of the operator and the rank of the corresponding interation; and

an element ~~(4)~~ for selecting one of the work registers to be associated with the operator.

2. The circuit of claim 1, wherein said function is a Hash function.

3. The calculation circuit of claim 1, wherein a multiplexer ~~(4)~~ forming the selection element is controlled by a priority decoder associated with an integrated processor containing said calculation circuit.